REMARKS

Applicants will address each of the Examiner's rejections in the order in which they appear in the Final Rejection.

Claim Rejections - 35 USC §102

Claims 11-18, 23-32 and 34-35

In the Final Rejection, the Examiner continues to reject Claims 11-8 [sic 18], 23-32 and 34-35 under 35 USC §103(a) as being unpatentable over Kern, "Handbook of Semiconductor Wafer Cleaning Technology", Science, Technology and Applications, Noyes Publication. Westwood, NJ, USA (1993). This rejection is respectfully traversed.

As Applicants explained in the Response to Office Action filed on March 31, 2005, Kern fails to disclose or suggest the claimed invention. Accordingly, for the reasons discussed in that response, Applicants continue to traverse this rejection and believe it should be withdrawn.

However, in order to advance the prosecution of this application, Applicants are amending independent Claims 11 and 15 to recite "forming a semiconductor film over a substrate having an insulating surface" and Claims 23 and 27 to recite "forming a gate wiring over a substrate having an insulating surface." While Kern discloses a semiconductor wafer and devices formed over a semiconductor wafer, Kern does not disclose or suggest a substrate (or wafer) having an insulating surface and a semiconductor film or gate wiring formed over the substrate having the insulating surface.

In addition, Applicants have amended independent Claims 11 and 15 to recite that the method comprises "forming a patterned resist mask over said semiconductor film;" patterning said

semiconductor film to form at least one semiconductor island;" "removing the patterned resist mask located over said semiconductor island;" and "spinning the substrate after removing the patterned resist mask." It is respectfully submitted that such features are not disclosed or suggested by Kern. Hence, these claims are clearly patentable thereover.

With regard to Claims 23 and 27, the Examiner argues that since Kern teaches the fabrication of various semiconductor devices, the wiring layer is inherent. However, Kern actually teaches devices formed over the semiconductor wafer in which a semiconductor layer is included. Therefore, it is not inherent in Kern to form a gate insulating film and a semiconductor film over the gate wiring formed over the substrate having an insulating surface.

Therefore, for at least the above-stated reasons, Claims 11-18, 23-32 and 34-35 of the present application are not disclosed or suggested by the cited reference and are patentable thereover. Accordingly, it is respectfully requested that this rejection be withdrawn.

Claims 19-22 and 36

The Examiner also rejects Claims 19-22 and 36 under 35 USC §102(b) as being anticipated by Chiyou et al. (JP 11-016866). This rejection is also respectfully traversed.

More specifically, the Examiner contends that Chiyou teaches forming at least one semiconductor island over said substrate by patterning the crystallized semiconductor film (citing Drawing 3 of Chiyou in support thereof). However, as Applicants previously explained, drawing 3 does not teach forming a semiconductor island. Instead, drawing 3 shows a water drop on an amorphous silicon surface (see 3A), or a water mark on an amorphous silicon surface (see 3B). See e.g. [0008] in Chiyou.

In order to make this clear, the Examiner's attention is direct to US 6,235,122 (Zhang et al.).

Previously, Applicants had submitted the '122 patent in an IDS on May 29, 2002 which the Examiner reviewed, initialed the 1449 but did not rely upon to reject the claims of the present application. See Office Action of July 5, 2002. As shown in Exhibit A (Family List of JP 11-016866 published by the EPO) attached herewith, US 6,235,122 is in the family of JP 11-016866. Once the Examiner has reviewed the '122 patent, it will be clear that Figs. 3, 3B do not teach forming at least one semiconductor island..., but teach a water drop or water mark. Hence, these figures are not relevant to the claimed invention.

The Examiner also contends in paragraphs 25-26 of the Final Rejection that the formation of semiconductor islands is inherent in Chiyou. Even if this is true, it is not clear from Chiyou as to when such a step is performed. In contrast, independent Claim 19 of the present application requires at least the steps of:

forming a semiconductor film;

crystallizing the semiconductor film;

forming a patterned resist mask;

patterning the crystallized semiconductor film to form at least one semiconductor island;

removing the patterned resist mask;

spinning the substrate after removing the patterned resist mask; and

applying an etching solution to a surface of said semiconductor island.

Chiyou, however, does not disclose or suggest these steps. Hence, independent Claim 19 and those claims dependent thereon are patentable over this reference. Accordingly, it is respectfully requested that this rejection be withdrawn.

New Claims

Applicants are adding new Claims 37-42 herewith. If any fee is due for these new claims, please charge our deposit account 50/1039.

Information Disclosure Statement

Applicants are filing an information disclosure statement (IDS) herewith. It is respectfully requested that this IDS be entered and considered prior to the issuance of any further action on this application.

Conclusion

Accordingly, the present application is in a condition for allowance and should be allowed.

Please charge Deposit Account No. 50-1039 for any fee due for this amendment.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: September 9, 2005

Mark J. Murphy
Registration No. 34,225

COOK, ALEX, McFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
200 West Adams Street
Suite 2850
Chicago, Illinois 60606
(312) 236-8500

Customer No. 000026568

Family list
4 family members for:
JP11016866
Derived from 3 applications.

1 **METHOD AND EQUIPMENT FOR CLEANING SILICON**
Publication info: JP11016866 A - 1999-01-22

2 **Cleaning method and cleaning apparatus of silicon**
Publication info: US6235122 B1 - 2001-05-22

3 **Cleaning method and cleaning apparatus of silicon**
Publication info: US6696326 B2 - 2004-02-24
US2002052096 A1 - 2002-05-02

Data supplied from the ***esp@cenet*** database - Worldwide

EXHIBIT A